EECS 2077 Test #3, Winter 2015 Name:_____

#1 ____/25 pts
#2 ____/30 pts
#3 ____/17 pts
#4 ____/28 pts

Allowed materials: 3 pages of 1-sided equation sheets, writing utensil, calculator.
Remember – we use cgs units! Centimeter/gram/second.
kT = 0.026 eV (300K) ε_0=8.854x10^{-14} F/cm ε_r(Si)=11.8 ε_r(SiO_2)=4.0
q= 1.6x10^{-19} C n_i(Si)=1.5x10^{10} / cm^3

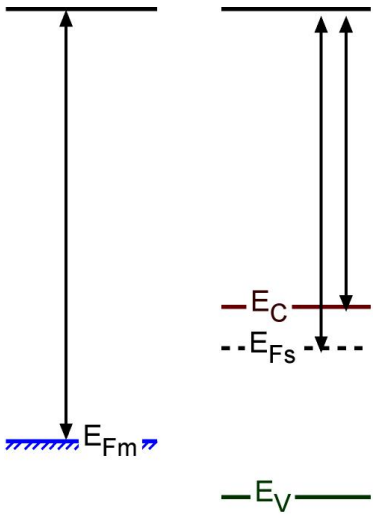
Prof. Heikenfeld will be out of town, so please read all problems carefully right away and he will try to be available to answer questions via text to 513-884-4094. If you want to text me, come up and do it in front of the test proctor (to make sure you are not texting answers back and forth with each other).

1.) [25 pts] A metal-semiconductor diode! Again! And again! As I noted, I tend to reintroduce problems that folks may have struggled with on previous tests.

(a) [9 pts] draw the resulting band diagram after the materials are contacted. Make sure you label the contact potential on your band diagram.

(b) [8 pts] redraw the diagram for forward bias, and draw with an arrow where the current is coming from.

(c) [8 pts] challenge problem :) Draw the E-field plot for this device for both the cases of no-voltage and forward-bias voltage (make sure you label which is which!).



2) [30 pts] Question related to an p-MOS transistor with the following parameters:

The gate electrode 'metal' is n+ poly Silicon.

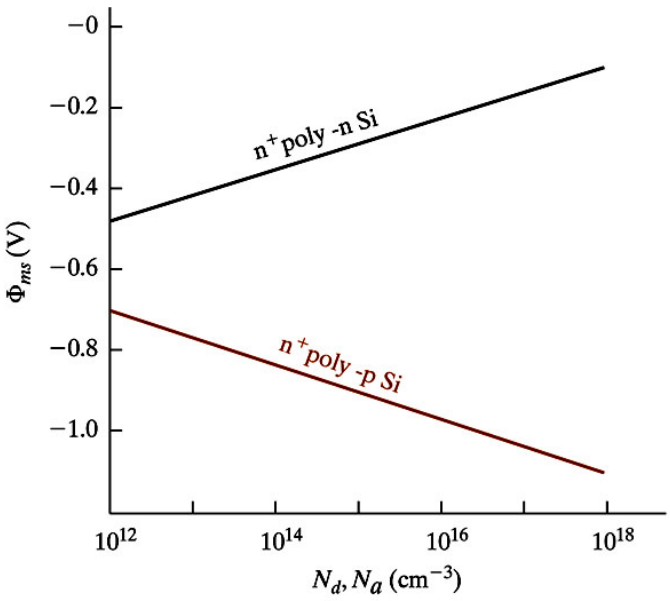
The substrate is doped with Phosphorus to the level of Nd=10^{16}/cm^3.

In the plot shown at right, the curves are labeled as 'gate material – substrate material'.

The gate oxide is has a thickness of 20 nm and a dielectric constant of 4.

There is an interface charge (Qi) of -50 nC/cm^2.

$$V_T = \phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_{D,\max}}{C_i} + 2\phi_f$$



a) provide the value for how much the Fermi level in the substrate has been shifted from the intrinsic Fermi level due to doping (deeper into the substrate, where the bands are flat) [5 pts]:

b) calculate the capacitance per unit area of the gate oxide [5 pts]:

c) provide the value for the maximum depletion charge [5 pts]

d) provide the value for how much threshold voltage is influenced by the fact that the Fermi level of the gate electrode and the Fermi level of the substrate Si, have to shift to match up at equilibrium [5 pts]:

e) calculate the threshold voltage for this device [10 pts]:

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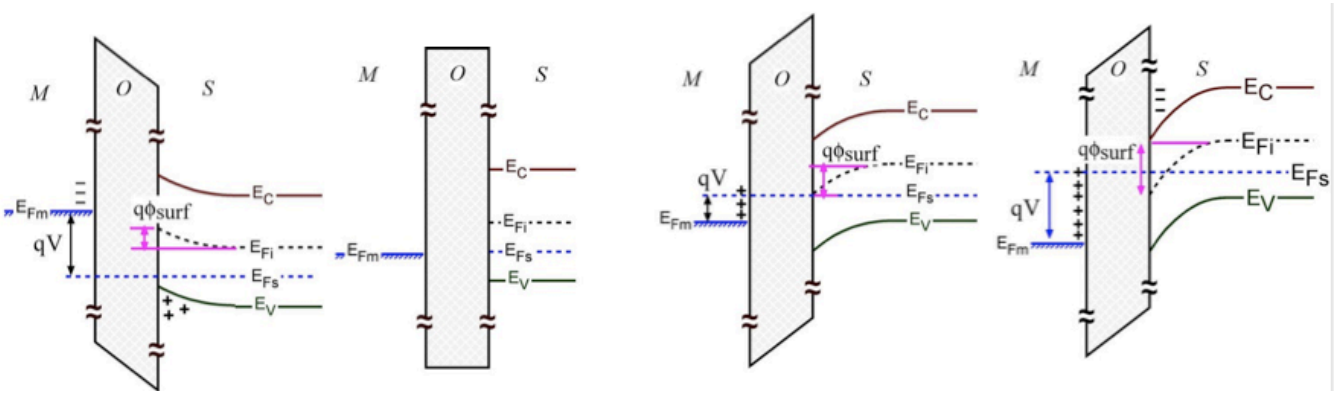
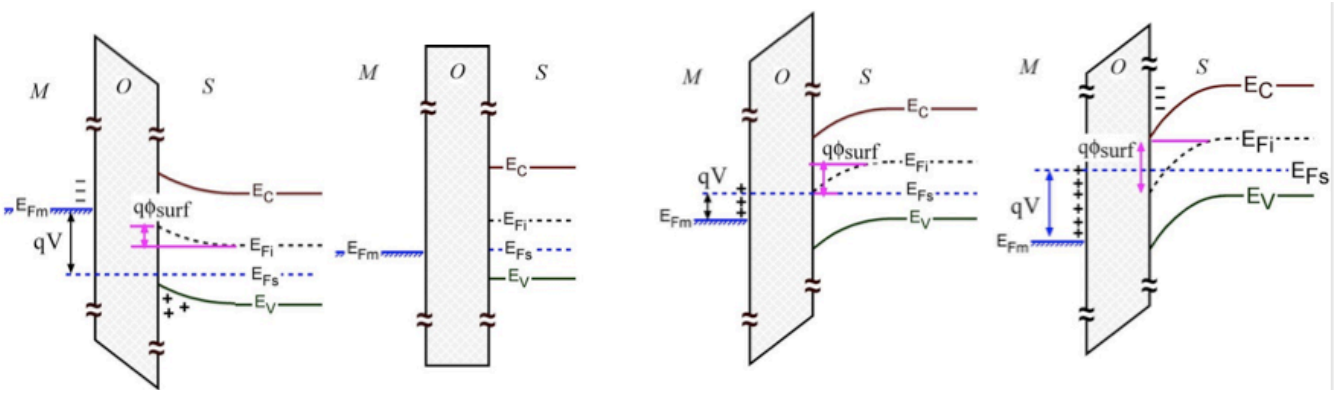
3) [17 pts] Mish-mash of MOSFET questions…

a) [4 pts] For the diagrams below, circle which states give <u>maximum current</u> from source to drain. If there are two or more states that are equal in the amount of maximum source to drain current, circle them.



b) [5 pts] For the diagrams below, circle which states give the <u>maximum</u> electrical impedance at the gate. If there are two or more states that are equal in the amount of maxim impedance, circle them.



c) [4 pts] Which has a higher input impedance for DC voltage signals? Circle one:

MOSFET, BJT, BOTH ARE SAME, NEITHER

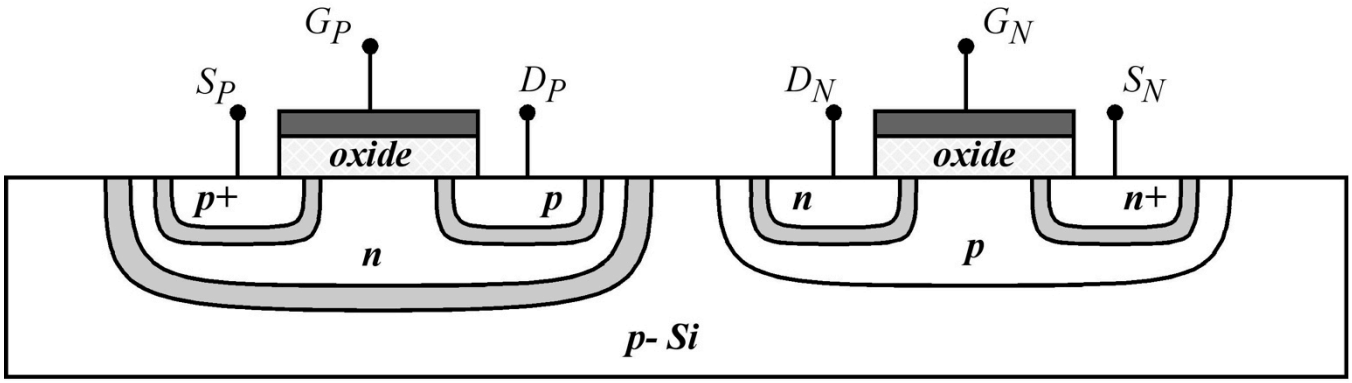
d) [4 pts] Circle the parts of the equation below that FLIP in polarity of voltage as you change from NMOS to PMOS.

$$V_T = \quad \phi_{ms} \quad -\frac{Q_i}{C_i} \quad -\frac{Q_{D,\max}}{C_i} \quad +2\phi_f$$

4.) [28 pts] The following is for an ideal pair of NMOS and PMOS devices that form the basis for a logic inverter. Perform the following. QUALITATIVE ANSWERS / NO EQUATIONS CALCULATIONS ARE NEEDED.

(a) FIRST: draw an input voltage (V_{IN}) that connects to both gates (G), draw an output voltage (V_{OUT}) that connects to both drains (D), draw a ground on the NMOS source and +5V on the PMOS source.

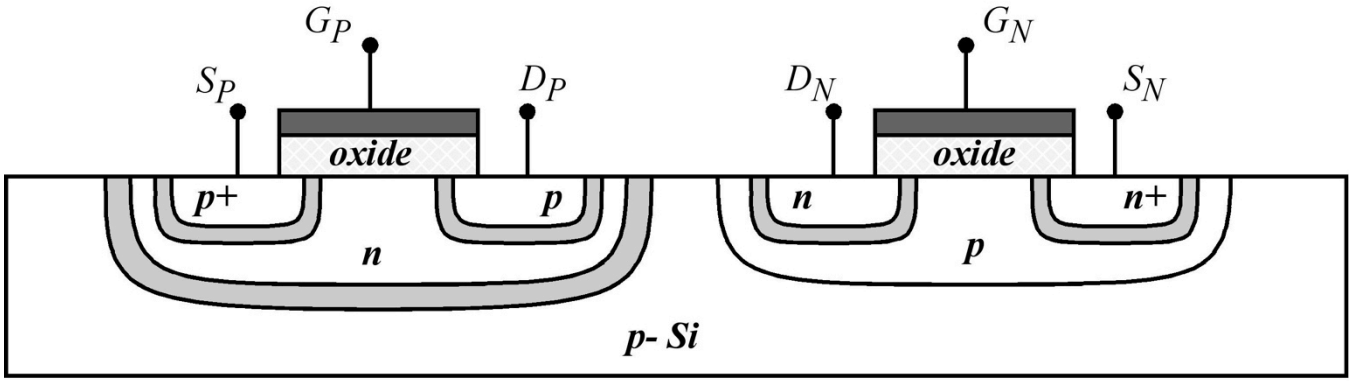
SECOND: using lines with arrows, or directly on the diagram, label as many voltages as possible on each semiconductor region (there are 7 different regions below, 2 points each) for the case of 0V applied to V_{IN}, and also label the voltage at V_{OUT} (just label the voltages at 0V, or 5V, and don't worry about labeling the voltages close to the gate oxide).



(b) Now, lets mix it up a bit…

FIRST: draw an input voltage (V_{IN}) that connects to both gates (G), draw an output voltage (V_{OUT}) that connects to both drains (D), draw -5V on the NMOS source and 0V on the PMOS source.

SECOND: label the diagram similar to how you did for part (a), but do it for the case where the output voltage is -5 V. Note, now you have to label the input voltage too! You may only label it with voltages such as --10V, -5 V, 0V, 5V, 10V. Do not use any more voltage than is needed to exceed Vth.



EXTRA SPACE